UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,907	03/30/2004	Christopher J. Diorio	IMPJ-0027A	5046

49684 7590 12/21/2005

THELEN REID & PRIEST LLP
IMPJ
P.O. BOX 640640
SAN JOSE, CA 95164-0640

EXAMINER	
PHAN, TRONG Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/813,907	DIORIO ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-117* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~2005~~. 3/36/04; 8/02/04; 2/10/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: **LOGIC in Figs. 3 and 13; S, G, D, fg0 and fg1 in Fig. 4; source, drain, p+, p- and n- in Fig. 5A; drain, source, Storage Transistor, Common Floating gate, n- and p- in Figs. 5B and 5D; drain, source, n+ and p- in Fig. 5C; drain, source, p+, p- and n- in Fig. 5E; drain, source, n+ and p- in Fig. 5F; latch_0, latch_1, fg0 and fg1 in Figs. 7-9; latch_0 and latch_1 in Fig. 10; 116 in Fig. 11; fg_0, fg_n, input_0, input_m in Figs. 12A and 16, fg0, p and n in Fig. 12B; fg0 in Fig. 12C; latchm_1 in Fig. 17; fg0, fg1, latch_0 and latch_1 in Fig. 18; fg0 and fg1 in Fig. 19; MOSCAP Tunneling Junction, conductor, V_tun, floating gate, n-, n+ and p- in Fig. 20; pFET Tunneling Junction, conductor, V_tun, floating gate, n+, n-, p- and p+ in Fig. 21; fg0 and fg1 in Fig. 23; Ai, Ai, HV-fg0 and HV-fg1 in Fig. 25; S0, FF, D and D in Fig. 27; HV_fg0, HV_fg1, latch_0 and latch_1 in Fig. 28; LOCOS or STI, gate oxide, electron injection, p- substrate, p-, p+, n-, n+ and electron tunneling in Fig. 29A; source metal, contact cut, n+ well contact, p+ source diffusion, p+ diffusion, p+ diffusion (shorted pFET), n- and n- well in Fig. 29B**. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the

immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: the serial number of the copending application as recited in lines 1-4, page 47 of the specification should be provided. Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-117 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-42 and 65-73 of copending Application No. 10/814,868. Although the conflicting claims are not identical, they are not patentably distinct from each other because the electronic fuse as recited in claims 1-117 of the present invention is read on each of the rewriteable electronic fuse as recited in claims 1-42 and 65-73 of copending Application No. 10/814,868.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. Claims 1-117 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-72 of copending Application No. 10/814,866. Although the conflicting claims are not identical, they are not patentably distinct from each other because the electronic fuse as recited in claims 1-117 of the present invention is read on the master fuse as recited in claims 14-72 of copending Application No. 10/84,866.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brice et al. 4,541,073, in view of Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456,992, Houston, 5,018,102, Naffziger et al., 6,363,006, and Bertin 4,158,239.

Brice et al. 4,541,073, discloses in Fig. 2 a nonvolatile memory device comprising:

I) Regarding claims 1-6, 11, 15, 19-24, 29, 33, 37-42, 47, 51, 55-58, 61-63, 68, 72, 76-79, 82-84, 89, 93, 97-100, 103-105, 110 and 114:

flip-flop 1, which can be used as a latch as well known in the art, comprising inverter T1/T2 being cross-coupled with inverter T3/T4;

nonvolatile memory element comprising first floating gate MOS transistor TM1 and second floating gate MOS transistor TM2 (see lines 60-64, column 3); wherein:

the two logical states of the flip-flop 1 being determined by the applied power-up supply VCC and the reset signal CR (see lines 33-35, column 5);

What is not shown in Brice et al. 4,541,073, is the fuse as recited in claims 1-6, 15, 19-24, 33, 37-42, 51, 55-58, 61-63, 72, 76-79, 82-84, 93, 97-100, 103-105 and 114 and the ultraviolet radiation exposure as recited in claims 11, 29, 47, 68, 89 and 110.

Eitan et al., 4,758,869, disclose the teaching that nonvolatile floating gate transistor can be used as a fuse (see lines 16-18, column 1).

Therefore, first floating gate MOS transistor TM1 and second floating gate MOS transistor TM2 would have been obvious considered as fuses as recited in claims 1-6, 15, 19-24, 33, 37-42, 51, 55-58, 61-63, 72, 76-79, 82-84, 93, 97-100, 103-105 and 114 as taught by Eitan et al., 4,758,869.

Eitan et al., 4,758,869, also discloses the teaching of using ultraviolet radiation exposure mechanism in nonvolatile memory device (see lines 63-67, column 3 and lines 39-53, column 5).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al. 4,541,073, by this teaching of Eitan et al., 4,758,869, for the purpose of erasing the first floating gate MOS transistor TM1 and the second floating gate MOS transistor TM2 in Fig. 2 of Brice et al., 4,541,073, as recited in claims 11, 29, 47, 68, 89 and 110.

II) Regarding claims 7-10, 25-28, 43-46, 64-67, 85-88 and 106-109:

What is not shown in Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, is the features as recited in claims 7-10, 25-28, 43-46, 64-67, 85-88 and 106-109.

Mehta, 6,214,666, discloses the teaching of using Fowler-Nordheim tunneling (see lines 6-7 and 41-42, column 2), hot electron injection (see lines 11-12 and 41-42, column 8), direct tunneling (see line 4, column 2) and hot hole injection (see lines 40-41, column 8) mechanism in nonvolatile memory device.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, by Mehta, 6,214,666, for the purpose of erasing the first floating gate MOS transistor TM1 and the second floating gate MOS transistor TM2 in Fig. 2 of Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, as recited in claims 7-10, 25-28, 43-46, 64-67, 85-88 and 106-109.

III) Regarding claims 12-13, 30-31, 48-49, 59-60, 69-70, 80-81, 90-91, 101-102 and 111-112:

What is not shown in Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, and Mehta, 6,214,666, is the capacitors coupled in common with the floating gate transistor as recited claims 12-13, 30-31, 48-49, 59-60, 69-70, 80-81, 90-91, 101-102 and 111-112.

Shibata et al., 6,456,992, discloses in Fig. 2B the teaching of coupling capacitors C1-C4 in common with the floating gate FG 206 of a nonvolatile memory cell MOS transistor.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, and Mehta, 6,214,666, by Shibata et al., 6,456,992, for the purpose of altering the potential value (see lines 28-42, column 5 of Shibata et al., 6,456,992) of the first floating gate MOS transistor TM1 and the second floating gate MOS transistor TM2 in Fig. 2 of Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, and Mehta, 6,214,666, as recited in claims 12-13, 30-31, 48-49, 59-60, 69-70, 80-81, 90-91, 101-102 and 111-112.

IV) Regarding claims 14, 16, 32, 34, 50, 52, 71, 73, 92, 94, 113 and 115:

What is not shown in Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, and Shibata et al., 6,456, 492, is the capacitor load coupled between an output of the latch and a fixed voltage source as recited claims 12-13, 30-31, 48-49, 59-60, 69-70, 80-81, 90-91, 101-102 and 111-112.

Houston, 5,018,102, discloses in Fig. 3 the teaching of coupling capacitor load 32 between the output node S1 and ground of a CMOS latch SRAM cell 2.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, and Shibata et al., 6,456,992, by Houston, 5,018,102, for the purpose of providing asymmetrical capacitance (see lines 30-36, column 3 of Houston, 5,018,102) at the output Q of flip-flop 1 in Fig. 2 of Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, and Shibata et al., 6,456,492, as recited in claims 14, 16, 32, 34, 50, 52, 71, 73, 92, 94, 113 and 115.

V) Regarding claims 17, 35, 53, 74, 95 and 116:

What is not shown in Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456, 492, and Houston, 5,018,102, is the first one of the cross-coupled inverters having at least one transistor with a gate-width-to-length that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of the cross-coupled inverters as recited claims 17, 35, 53, 74, 95 and 116.

Naffziger et al., 6,363,006, discloses in Fig. 2 Prior Art a cross-coupled inverter SRAM cell having the gate width of transistors 32 and 34 being larger than the gate width of transistors 26 and 28 (see Table 1 in column 4).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al., 4,541,073, which is

modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456,992, and Houston, 5,018,102, by Naffziger et al., 6,363,006, for the purpose of providing a faster bit slew read rate (see lines 22-24, column 3 of Naffziger, 6,363,006) for the flip-flop 1 In Fig. 2 of Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456,492, and Houston, 5,018,102, as recited in claims 17, 35, 53, 74, 95 and 116.

VI) Regarding claims 18, 36, 54, 75, 96 and 117:

What is not shown in Brice et al. 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456, 492, Houston, 5,018,102, and Naffziger et al., 6,363,006, is the channel doping level of one transistor of the first one cross-coupled inverter being different from the channel doping level of one transistor of the second one of the cross-coupled inverter as recited claims 18, 36, 54, 75, 96 and 117.

Bertin, 4,158,239, discloses the teaching of making the gate-width-to-length ratio and channel doping level of the transistors forming the flip-flop to be different from one to another (see lines 4-9, column 4).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata et al., 6,456,992, Houston, 5,018,102, and Naffziger et al., 6,363,006, by Bertin, 4,158,239 for the purpose of achieving an asymmetrical state for the flip-flop 1 in Fig. 2 of Brice et al., 4,541,073, which is modified by Eitan et al., 4,758,869, Mehta, 6,214,666, Shibata

et al., 6,456,492, Houston, 5,018,102, and Naffziger et al., 6,363,006, as recited in claims 18, 36, 54, 75, 96 and 117.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roohparvar et al., 6,141,247, Hirose et al., 6,363,011, Murray, 6,469,930, and Santin et al., 6,845,029.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phan Trong

TRONG PHAN
PRIMARY EXAMINER